2023
DESIGN AND VERIFICATION™
DVCON
CONFERENCE AND EXHIBITION
UNITED STATES

SAN JOSE, CA, USA
FEBRUARY 27-MARCH 2, 2023

DVCON 2023 UNITED STATES CONFERENCE PROGRAM

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dvcon.org

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DVCon U.S. 2023

Welcome Message from DVCon U.S. General Chair, Vanessa Cooper

General Chair – Vanessa Cooper, Verilab, Inc.

I am pleased to welcome you to the DVCon U.S. 2023 conference and exhibition! This is our first year back to an in-person conference, and I extremely excited to see everyone in person. Attendees can look forward to outstanding technical sessions and discussions on many hot topics, as well as networking during the breakout sessions and receptions, and opportunities to preview the latest industry design and verification tools and services from the best in the industry.

We are proud of continuing our tradition of providing an annual technical forum that serves the needs of the practicing design and verification community, organized by dedicated volunteers from the community itself.

Now in its 35th year, DVCon U.S. has established itself as the must-attend industry and user-focused conference for design and verification engineers, EDA developers, IP integrators and design managers, focusing on design and verification of electronic systems and integrated circuits. We are proud that this conference attracts wide participation from the industry from the smaller to the larger companies throughout the program and exhibition.

Our four-day virtual program contains many key design and verification topics including RISC-V, cloud-based design, open source, formal verification, portable stimulus, IP security, UVM, functional safety, prototyping and emulation, SystemC, and many others. The event provides an opportunity to discuss challenges and solutions that can be beneficial in current and upcoming projects as electronic designs and verification complexities and challenges continue to increase exponentially. Attendees will find each of these areas addressed at the conference's sessions, panels, posters, tutorials, and short workshops with an emphasis on solutions to engineers' real-world problems.

We are pleased to offer attendees an in-depth technical program with a wide variety of choices. We received numerous outstanding submissions for papers, panels, tutorials, and short workshops from the best technical minds and organizations in the industry. Our focus on the users of Accellera standard EDA languages, tools, and methodologies continues to be a DVCon 2023 hallmark. Attendees can expect to learn about both practical solutions to their pressing problems and preview the technologies that will affect them in the near future.

I am pleased to present the work of the DVCon Steering Committee and Technical Program Committee, who have put together an excellent 2023 program with the support of our conference management specialists, Conference Catalysts.

Highlights of the conference include:

Accellera Day: On Monday, February 27, our conference sponsor, Accellera Systems Initiative, kicks off DVCon U.S. with Accellera Day. We will have a morning Accellera tutorial on the Portable Stimulus standard, as well as three Accellera short workshops presented by Accellera standards working group members throughout the day. We will have four sponsored short workshops in the afternoon presented by design verification industry members covering topics such as Mixed-Signal verification, power efficient systems, formal verification, and more.

Keynote: This year's keynote, "What Do Farming, Steel, and Space Have in Common," will be given by Dr. Dirk Didascalou, Chief Technology Officer at Siemens Digital Industries. In his presentation, Dr. Didascalou will discuss how discuss how digitalization is driving transformations in every part of life.

Technical papers and posters: Technical Program Chair, Josh Rensch, and Poster Chair, Tom Fitzpatrick, have organized an excellent technical program on Tuesday and Wednesday that includes papers and a new format for the Poster session. The Poster Ninja Warrior session will include four posters that will battle it out, with each presenter given five minutes to deliver.

We are very grateful for the outstanding submissions and the work done by the technical program committee volunteers to review the submissions and encourage the community to keep submitting. There are so many good choices that you will want to go through the program and review it thoroughly as you plan each day. There is something for everyone in this broad, in-depth technical program. With so many interesting options, we look forward to your votes for the best paper and best poster awards after the last program session on Wednesday.

Tutorials and Short Workshops: Xiaolin Chen, Tutorial and Short Workshop Chair, has put together an outstanding selection of tutorials and short workshops for Monday and Thursday. The short workshops are extremely popular and are intended to give more organizations, mostly smaller companies, greater opportunity to participate in the program and give attendees more variety in shorter educational and learning sessions. We have sponsored short workshops in this year's program, on Monday and Thursday, covering a wide variety of topics.

We will have two sponsored tutorials on Thursday with topics covering: Effective Verification Management and XMODEL.

Panels: Ambar Sarkar, Panel Chair, has organized two interesting and thought-provoking panel sessions: "Systems are Evolving. Is Verification Keeping Up?" and "AI-ML Algorithms are Transforming Verification: Separating Hype from Reality." Both panels will offer attendees an opportunity to ask questions during a live Q&A on the conference platform.

We invite all attendees to visit the Exhibition floor. It is an excellent way to connect with colleagues as well as learn about the latest products in the design and verification industry.

My sincere thanks to our program sponsor, Accellera Systems Initiative, industry sponsors, steering committee volunteers, technical program committee volunteers, past chairs and Conference Catalyst staff who have worked hard to put together a program that makes DVCon "the" conference for design and verification engineers.

I sincerely look forward to seeing you DVCon U.S. 2023!

Vanessa Cooper
DVCon U.S. 2023 General Chair

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Accellera Systems Initiative is an independent, not-for profit organization dedicated to create, support, promote, and advance system-level design, modelling, and verification standards for use by the worldwide electronics industry. We are composed of a broad range of members that fully support the work of our technical committee to develop technology standards that are balanced, open, and benefit the worldwide electronics industry. Leading companies and semiconductor manufacturers around the world are using our electronic design automation (EDA) and intellectual property (IP) standards in a wide range of projects in numerous application areas to develop consumer, mobile, wireless, automotive, and other "smart" electronic devices. Through an ongoing partnership with the IEEE, standards and technical implementations developed by Accellera Systems Initiative are contributed to the IEEE for formal standardization and ongoing governance.

Our Mission

At Accellera our mission is to provide a platform in which the electronics industry can collaborate to innovate and deliver global standards that improve design and verification productivity for electronics products.

The purposes of the organization include:

- Provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process.
- Collaborate with our community of companies, individuals, and organizations to deliver standards that lower the cost of designing commercial IC and EDA products and embedded system solutions, as well as increase the productivity of designers worldwide.
- Encourage availability and adoption of next-generation EDA and IP standards that encompass system-level, RT-level, and gate-level design flows.
- Collaborate with the electronic design community to deliver standards that increase designer productivity and lower the cost of product development.
- Provide mechanisms that enable the continued growth of the Accellera Systems Initiative user community including SystemC, Universal Verification Methodology (UVM), and IP-XACT.
- Standardize technical implementations developed by Accellera Systems Initiative through the IEEE.

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DVCon U.S. 2023 - Program Grid
27 FEBRUARY 2023

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<tr><th>TIME (PST)</th><th>Monterey Carmel</th><th>Oak</th><th>Fir</th><th>Bayshore Ballroom</th></tr>
<tr><td>9:00 - 10:30</td><td>What is new in IP-XACT IEEE Std. 1685-2023?
accellera SYSTEMS INITIATIVE</td><td>Pushbutton Complete IP Generation
AGNISYS SYSTEM DEVELOPMENT WITH CERTAINTY</td><td rowspan="3">User Experiences with the Portable Stimulus Standard
accellera SYSTEMS INITIATIVE</td><td rowspan="8">Exhibitor Set Up
(12:00 – 16:00)</td></tr>
<tr><td>10:30 - 11:00</td><td colspan="2">Coffee Break
(Gateway Foyer)</td></tr>
<tr><td>11:00 - 12:30</td><td>Applications of the UVM-AMS Standard
accellera SYSTEMS INITIATIVE</td><td>Static Signoff Best Practices – Learnings and experiences from industry use cases
REAL INTENT</td></tr>
<tr><td>12:30 - 13:30</td><td colspan="3">Lunch Sponsored by:
accellera SYSTEMS INITIATIVE
The CHIPS Act and Its Impact on the Design & Verification Markets
(Pine Cedar)</td></tr>
<tr><td>13:30 - 15:00</td><td>Hardware/Software Interface Formats – A Discussion
Semifore An Arteris Business</td><td>A Methodology for Power and Energy Efficient Systems Design
SIEMENS</td><td rowspan="3">The Next Frontiers of Formal Verification
SYNOPSYS®</td></tr>
<tr><td>15:00 - 15:30</td><td colspan="2">Coffee Break
(Gateway Foyer)</td></tr>
<tr><td>15:30 - 17:00</td><td>IEEE 1666-202x SystemC Sneak Peek
accellera SYSTEMS INITIATIVE</td><td>Democratizing digital-centric mixed-signal verification methodologies
SIEMENS</td></tr>
<tr><td>17:00 - 18:30</td><td colspan="4">Welcome/Exhibitor Reception
(Bayshore Ballroom)</td></tr>
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DVCon U.S. 2023 - Program Grid
28 February 2023

TIME (PST)	Monterey Carmel	Oak	Fir	Bayshore Ballroom
8:00 - 8:30	**Opening Session** (Oak)			
8:30 - 9:00	**Coffee Break** (Gateway Foyer)			**Exhibit Hall Open** (13:30-18:00)
9:00 - 11:00	**Assimilate Machine Learning**	**Configuring UVM**	**Controlling UPF**	
11:00 - 12:30	**Poster Session** (Gateway Foyer)			
12:30 - 13:30	**Lunch Sponsored by** SIEMENS A Data-Driven Escape from the Verification Pit of Despair (Pine Cedar)			
13:30 – 14:30	**Keynote: Dirk Didascalou** (Oak / Fir)			
14:30 – 15:00	**Coffee Break** (Gateway Foyer)			
15:00 – 17:00	**Formal Restrained**	**Process RISC_V**	**Systematic Methodology**	

DVCon U.S. 2023 - Program Grid
1 March 2023

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<tr><th>TIME (PST)</th><th>Monterey Carmel</th><th>Oak</th><th>Fir</th><th>Bayshore Ballroom</th></tr>
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(Oak/Fir)</td><td rowspan="11">Exhibit Hall Open
(13:30 – 18:30)</td></tr>
<tr><td>9:00 - 9:30</td><td colspan="3">Coffee Break
(Gateway Foyer)</td></tr>
<tr><td>9:30 – 11:00</td><td>Discovering Formal</td><td>Constraining Constraints</td><td>Completing Coverage</td></tr>
<tr><td>11:00 – 12:00</td><td colspan="3">Poster Ninja Warrior
(Oak)</td></tr>
<tr><td>12:00 – 13:30</td><td colspan="3">Lunch Sponsored by:
accellera SYSTEMS INITIATIVE
Brief update on Accellera working group activities, followed by an invited talk: “RISC-V Everywhere”
(Pine Cedar)</td></tr>
<tr><td>13:30 – 14:30</td><td colspan="3">Panel: AI-ML Algorithms are Transforming Verification: Separating Hype from Reality
(Oak / Fir)</td></tr>
<tr><td>14:30 – 15:00</td><td colspan="3">Coffee Break
(Gateway Foyer)</td></tr>
<tr><td>15:00 – 16:30</td><td>Analog/Mixed Signal Snorgasbord</td><td>Protecting Safety and Security</td><td>UVM Buffet</td></tr>
<tr><td>16:30 – 17:00</td><td colspan="3">Break</td></tr>
<tr><td>17:00 – 17:30</td><td colspan="3">Best Paper Presentation
verilab
(Bayshore Ballroom)</td></tr>
<tr><td>17:30 – 18:30</td><td colspan="3">Exhibitor Reception
(Bayshore Ballroom)</td></tr>
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DVCon U.S. 2023 - Program Grid
2 March 2023

TIME (PST)	Cascade	Donner	Siskiyou
9:00 – 10:30	**Verification 2.0 – Multi-Engine, Multi-Run AI-Driven Verfication** cadence®	**Accelerate Coverage Closure from Day-1 with AI-driven Verification** SYNOPSYS®	**Evolutionary and Revolutionary Innovation for Effective Verification Management & Closure** SIEMENS
10:30 – 11:00	**Coffee Break** (Bayshore Foyer)		
11:00 – 12:30	**A Wholistic Approach to Optimizing Your System Verification Flow** cadence®	**Growing need for End-to-end Protocol Verification Solutions from IP to Multi-die Systems** SYNOPSYS®	
12:30 – 13:30	**Lunch Sponsored by:** accellera SYSTEMS INITIATIVE UVM 1800.2-2020-2.0 Library Discussion (Sierra)		
13:30 – 15:00	**Understanding the RISC-V Verification Ecosystem** imperas	**Verification of Inferencing Algorithm Accelerators** SIEMENS	**Harnessing the Power of UVM for AMS Verification with XMODEL** scientific analog
15:00 – 15:30	**Coffee Break** (Bayshore Foyer)		
15:30 – 17:00	**Virtio based GPU Modeling** Vayavya Labs	**Getting Beyond ISA Compliance: Advanced Core/ SoC Verification for RISC-V and other Beasts** BREKER™	

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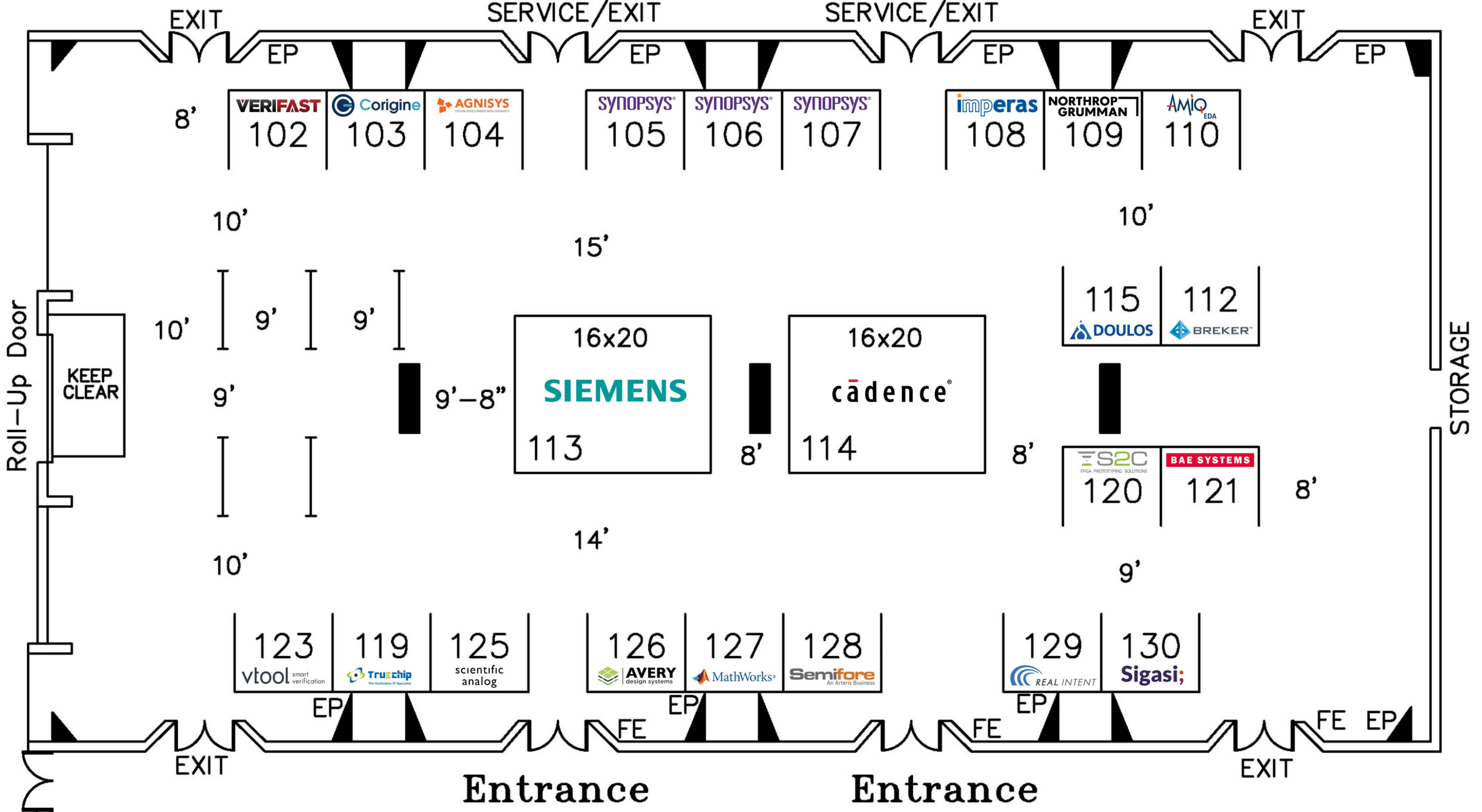
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Technical Program: Monday, February 27
Time Zone is PST

9:00–12:30
Tutorial: User Experiences with the Portable Stimulus Standard
Room: Fir
Presented by members of Accellera System Initiative

By: **Jonathan Edwards,** Intel; **Prabhat Gupta,** AMD

Abstract: The Accellera Portable Stimulus Standard is moving beyond the "bleeding edge." As the Portable Stimulus Working Group continues to develop additional features of the language, many companies are adopting the standard in their verification flows. This technical tutorial will begin with an overview of the new features to be included in the coming update to the standard and will feature users from AMD and Intel who will share their experiences using this exciting new technology.

9:00–10:30
Workshop: What is new in IP-XACT IEEE Std. 1685-2022?
Room: Monterey Carmel
Presented by members of Accellera System Initiative

By: **Richard Weber,** Semifore, an Arteris company; **Edwin Dankert,** Arm

Abstract: Accellera's IP-XACT Working Group has been developing a proposal for a revision of IEEE Std. 1685-2014. The proposal was handed over to the IEEE P1685 Working Group in late 2021 and was approved by IEEE Standards Association Board in September of 2022.

This workshop addresses the IP-XACT user community including IP and SoC companies, EDA vendors, and research institutes to inform them about upcoming changes in IEEE Std. 1685. It also addresses examples of commercial tool support for these changes.

9:00–10:30
Workshop: Pushbutton Complete IP Generation
Room: Oak
Presented by Agnisys

By: **Freddy Nunez,** Agnisys

Abstract: In IP/SoC design development, after capturing the register specification, the designers work on creating a synthesizable hardware application logic layer for their intended design functionality using the addressable hardware registers.

In this workshop, we plan to show how to automatically create that synthesizable application logic layer along with its RAL and AI based uvm tests for completely automating the development at the lower levels of the layered SoC/IP design development.

10:30 – 11:00
Coffee Break
Room: Gateway Foyer

Technical Program: Monday, February 27 (cont.)
Time Zone is PST

11:00 – 12:30
Workshop: Applications of the UVM-AMS Standard
Room: Monterey Carmel
Presented by members of Accellera System Initiative

By: **Tom Fitzpatrick,** Siemens EDA, UVM-AMS Working Group Chair;
Tim Pylant, Cadence Design Systems

Abstract: The Accellera UVM-AMS Standard will define an architecture and methodology to extend UVM testbenches from digital-only applications to DMS/real-number and AMS designs as well. This technical workshop will walk the audience through a worked example that will illustrate the key pieces of this approach and give a preview of how this standard will expand the ecosystem for AMS verification to allow vendors and users to create and share compatible verification components and use them in existing UVM environments.

11:00 – 12:30
Workshop: Static Signoff Best Practices – Learnings and experiences from industry use cases
Room: Oak
Presented by Real Intent

By: **Vikas Sachdeva,** Real Intent

Abstract: The tutorial covers the still-growing role of formal and static methods in various areas of front-end design: microarchitecture and functional correctness; clocks, resets, and metastability; and analog/mixed-signal verification. First, it contrasts Static verification with Dynamic verification. Next, it proposes when to use static methods based upon learnings from multiple industry use cases. It then details case studies and experiences and how to tame the problems that cause most of the design re-spins, namely logic and functional bugs, clocks and reset issues.

12:30 – 13:30
Lunch Sponsored by Accellera System Initiative
The CHIPS Act and Its Impact on the Design & Verification Markets
Room: Pine Cedar
Presented by Bob Smith Executive Director, SEMI ESD Alliance

Abstract: The CHIP Act is in the news constantly, yet most of the focus around it is on building domestic semiconductor manufacturing capability. This talk will address the basics of the CHIPS Act with an emphasis on understanding how it might impact and/or benefit the design and verification markets.

13:30 – 17:00

Tutorial: The Next Frontiers of Formal Verification
Room: Fir
Presented by Synopsys

By: **Ravindra Aneja,** Synopsys

Abstract: It's taken a few decades for formal verification to expand beyond a tool reserved for the select few with a Ph.D. to become a mainstream verification solution. In recent years, formal adoption has compounded due to the following trends:

- Ever-increasing design complexity affecting verification closure, making formal verification a must-have strategy in the overall verification flow;
- Formal applications targeting well-defined domains do not require formal expertise, such as reachability analysis, connectivity checking, control register verification, and X-propagation;
- Advanced formal applications, such as functional safety, security, low power, are expanding usage to critical design and verification problems;
- The role of machine learning to increase performance and capacity of the formal engines enabling its use for larger and highly complex designs;
- Leveraging the cloud to scale the use of formal methods across thousands of CPU cores.

Formal verification is like a diamond in the rough with exceptional potential to become as widely used as functional simulation. In this tutorial, attendees will learn about the advanced formal applications and hear first-hand what lies ahead, such as:

- Solving complexity challenges using advanced formal techniques
- Using formal methods to detect security leak at the SoC level
- The advantage to using formal for architectural verification
- Verifying the most complex datapath blocks, such as wide floating point math functions
- The need for model checking C/C++ models
- And more …

Attendees will walk away with a comprehensive understanding of advanced formal technologies and how to apply them across IP/block, subsystem, and SoCs.

13:30 – 15:00

Workshop: Hardware/Software Interface Formats – A Discussion
Room: Monterey Carmel
Presented by Semifore, an Arteris company

By: **Rich Weber, Jamsheed Agahi, Josh Rensch, and Eric Sherk,** Semifore, an Arteris company

Abstract: What format should we use to input address maps and registers? From spreadsheets to industry formats for specifying register and address map information, combined with widely differing uses of that information across the team, it can be overwhelming trying to decide what to do. Can we pull the register information from RTL or use the UVM-RAL definition? What is IP-XACT? Let's use spreadsheets, everyone understands those! A single source of truth for specifying the HSI that is persistent throughout the design process is essential for success.

In this short workshop, we will showcase the various industry standards and input formats around registers and the hardware/software interface (HSI). We will discuss the strengths and the shortcomings of these options. We will discuss which ones make sense for authoring HSI and which ones should be generated.

Technical Program: Monday, February 27 (cont.)

Time Zone is PST

9:00–10:30

Workshop: A Methodology for Power and Energy Efficient Systems Design

Room: Oak

Presented by Siemens EDA

By: **Mohammed Fahad,** Siemens EDA

Abstract: Power is everywhere. Traditionally, power used to be a concern with mobile and handheld devices due to battery life considerations. But now, power as a concern is prevalent in all verticals of the industry, for example, data centers consume huge amounts of power due to million of data transactions happening per second. Processors like CPUs and GPUs have always been power hungry but now with increased tiles and cores on these processors, the speeds are increasing manifolds which as result means significant rise in power dissipation. With 5G, edge computing and IoT, the devices are becoming compute intensive leading to more power consumption. And last but not the least, automotive. In cars, there is now a lot more electronics than it used to be, consuming a lot of power and generating a lot of heat.

In this workshop, I will be demonstrating why early RTL power and energy estimations are key metrics and how the two metrics have taken a center stage lately in performance-sensitive system design considerations. I will be talking about the RTL Power Analysis as a solution and the challenges associated with it. Also, I would be proposing a regression-ready, error-correcting and fully seamless methodology for an early Power closure at RTL level. I will discuss the key aspects of this methodology like With ever-increasing chip design complexity, including chips for domain-specific applications, the role of on-chip and off-chip protocols.

15:00 – 15:30

Coffee Break

Room: Gateway Foyer

15:30 – 17:00

Workshop: IEEE 1666-202x SystemC Sneak Peek

Room: Monterey Carmel

Presented by members of Accellera System Initiative

By: **Jerome Cornet,** IEEE P1666 Working Group Chair

Abstract: The next revision of IEEE 1666 SystemC is coming! It builds on enhancements and features contributed by the SystemC community during the last decade through the Accellera SystemC Language Working Group. This workshop will present some of the features of the upcoming revision, which modernize the language and enable new use cases.Target audience of this short workshop are system engineers, designers and architects who are familiar with SystemC simulation and modeling concepts, and would like to know which new capabilities are being introduced to enable efficient Electronic System Level (ESL) design, systems modeling or virtual prototyping in SystemC.

15:30 – 17:00

Workshop: Democratizing digital-centric mixed-signal verification methodologies

Room: Oak

Presented by Siemens EDA

By: **Sumit Vishwakarma,** Siemens EDA

Abstract: A mixed-signal design is a combination of tightly interlaced analog and digital circuitry. Next-generation automotive, imaging, IoT, 5G, computing, and storage markets are driving the strong demand for increasing mixed-signal content in modern systems on chips (SoCs). Chips are getting bigger, better, and more sophisticated. As designs complexity has multiplied, verification complexity has exploded The "Shift Left" trend has been around for over a decade. The idea is to verify early in the design cycle resulting in better products, fewer re-spins, faster time to market, and lower cost. Shift Left is driving the adoption of new verification methodologies. However, when it comes to mixed-signal designs, it gets a bit complicated due to the complexity of interactions between analog and digital.

Digital verification methodologies are mature, structured, and have mastered the art of automation. Analog verification, on the other hand, traditionally relied on direct verification methods. While this might have been sufficient in the past, growing design size and complexity require more comprehensive and automated verification of mixed-signal SoCs. The advent of new digital verification technologies — such as constrained-random data generation, assertion-based verification, coverage-driven verification, formal model checking, and Intelligent Testbench Automation to name a few — have changed the way we see functional verification productivity.

Analog verification teams must go beyond traditional approaches like directed tests, sweeps, corners, and Monte Carlo analysis. Teams need to adopt digital verification techniques to enable regression testing of mixed-signal SoCs. These techniques include automated stimulus generation, real number modeling, coverage, and assertion-driven verification combined with low-power verification and automated debug.

Most of these advanced new technologies have not been extended to verify mixed-signal design challenges. This could be due to a lack of knowledge, lack of standards, or lack of EDA technologies to support these methodologies in the mixed-signal domain. Typically, digital verification engineers use a top-down methodology while analog designers use a bottom-up approach. Recognizing the advantages of a top-down methodology, there is a paradigm shift happening to adopt it for analog and mixed-signal designs. In this workshop, we will discuss these digital-centric mixed-signal verification methodologies to improve SoC verification throughput and improve time to market. The session will include a presentation, a live demo, and Q&A.

17:00 – 18:30

Reception

Room: Bayshore Ballroom

Technical Program: Tuesday, February 28
Time Zone is PST

8:00 – 8:30

Opening Session
Room: Oak

8:30 – 9:00

Coffee Break
Room: Gateway Foyer

9:00 – 11:00

Assimilate Machine Learning
Room: Monterey Carmel
Session Chair: **Harry Foster**

Identifying unique power scenarios with advanced data mining techniques as full SoC (System On Chip) level with real workloads
Amir Attarha, Siemens; **Pankaj Chauhan,** Siemens; **Satish-Kumar Agrawal,** Siemens; **Gaurav Saharawat,** Siemens; **Diwakar Agrawal,** Siemens

A Survey of Machine Learning Applications in Functional Verification
Dan Yu, Siemens EDA; **Harry Foster,** Siemens EDA; **Tom Fitzpatrick,** Siemens EDA

Exploring Machine Learning to assign debug priorities to improve the design quality
Vyasa Sai, Intel Corporation; **Vaibhav Gupta,** Intel Corporation; **Fylur Rahman Sathakathulla,** Intel Corporation

9:00 – 11:00

Configuring UVM
Room: Oak
Session Chair: Paul Marriott

The Untapped Power of UVM Resources and Why Engineers Should Use the uvm_resource_db API
Clifford Cummings, Paradigm Works, Inc.; **Heath Chambers,** HMC Design Verification; **Mark Glasser,** Cerebras

Avoiding Configuration Madness The Easy Way
Rich EDELMAN, Siemens EDA

Tree Data Framework for Code Generation: Application of Generating UVM Testbench for Complex Designs
Chenhui Huang, Tenstorrent Inc.; **Yu Sun,** Tenstorrent Inc.; **Divyang Agrawal,** Tenstorrent Inc.

Strategies to Maximize Reusability of UVM Test Scenarios in SoC Verification
Hyeonman Park, Samsung Electronics; **Namyoung Kim,** Samsung Electronics; **Kyoungmin Lee,** Samsung Electronics

Technical Program: Tuesday, February 28 (cont.)
Time Zone is PST

9:00 – 11:00

Controlling UPF
Room: Fir
Session Chair: Amit Srivastav

Hierarchical UPF Design – The 'Easy' Way
Brandon Skaggs, Cypress Semiconductor, An Infineon Technologies Company; **Chris Turman,** Cypress Semiconductor, An Infineon Technologies Company; **Joe Whitehouse,** Cypress Semiconductor, An Infineon Technologies Company

Automation for Early Detection of X-propagation in Power-Aware simulation verification Using UPF IEEE 1801
Tony Gladvin George, Ramesh Kumar, Kyuho Shim, Karan K, Wooseong Cheong, Byung Chul Yoo - Samsung Electronics

Power Models & Terminal Boundary: Get your IP Ready for Low Power
Progyna Khondkar, Cadence Design Systems; **William Winkeler,** Cadence Design Systems; **Brandon Skaggs,** Infineon Technologies

Successive Refinement of UPF Power Switches
Prabhakar S Ayyagari, Intel Corporation; **William G Crocco,** Intel Corporation

11:00 – 12:30

Poster Session
Room: Gateway Foyer

#1: A Study on Virtual Prototyping based Design Verification Methodology
Woojoo Kim, Samsung Electronics; **Kunhyuk Kang,** Smasung Electronics; **Seonil Brian Choi,** Samsung Electronics

#2: A UVM Reactive Testbench for Jitter Tolerance Measurement of High-Speed Wireline Receivers
Jaeha Kim, Seoul National University

#3: Accelerated Verification of NAND Flash Memory using HW Emulator
Seyeol Yang, Samsung Electronics; **Byungwoo Kang,** Samsung Electronics; **Dongeun Lee,** Samsung Electronics; **Jintae Kim,** Samsung Electronics

#4: Accelerating Functional Verification through Stabilization of Testbench Using AI/ML
Srikanth Vadanaparthi, Qualcomm; **Pooja Ganesh,** Qualcomm; **Dharmesh Mahay,** Synopsys; **Malay Ganai,** Synopsys

#5: An Enhanced DV Approach for Effectively Verifying High Speed, Low Power MIPI-MPHY5.0 Designs
Eldhose PM, Samsung Semiconductor India Research; **Suraj Shetty,** Samsung Semiconductor India Research; **Sagar Jayakrishnan,** Samsung Semiconductor India Research; **Kuntal Pandya,** Samsung Semiconductor India Research; **Parag S. Lonkar,** Samsung Semiconductor India Research

#6: Automated Connectivity Test Creation for System-in-Package Analog Mixed-Signal Verification
Samantha Pandez, Analog Devices, Inc.; **Christopher Geen,** Analog Devices, Inc.

#7: Automation Methodology for Bus Performance Verification using IP-XACT
Taeyoung Jeon, Samsung Electronics; **Gunseo Koo,** Samsung Electronics; **Youngsik Kim,** Samsung Electronics; **Seonil Brian Choi,** Samsung Electronics

#8: Check Low-Power Violations by Using Machine Learning Based Classifier
Chi-Ming Lee, Mediatek; **Chung-An Wang,** Mediatek; **Cheok-Yan Goh,** Mediatek; **Chia-Cheng Tsai,** Mediatek; **Chien-Hsin Yeh,** Mediatek; **Chia-Shun Yeh,** Mediatek; **Chin-Tang Lai,** Mediatek

11:00 – 12:30

Poster Session (cont.)
Room: Gateway Foyer

#9: Discover Over-Constraints by Leveraging Formal Tool
Dongsheng Ouyang, NVIDIA Corporation; **Ray Zhang,** NVIDIA Corporation; **Lucus Liu,** NVIDIA Corporation; **Doris Yin,** NVIDIA Corporation; **Wayne Ding,** NVIDIA Corporation

#10: Do not forget to get your SystemC code covered with UVMC
Vishal Baskar, Siemens Industry Software Inc- Siemens EDA

#11: Improvement of UVM Scenario Generation, Control and Reproducibility using Portable Stimulus (PSS) for IP Validation
Robert Martin, Intel Corporation; **Alan Curtis,** Intel Corporation; **Gopinath Narasimhan,** Synopsys; **Qingwei Zhou,** Intel

#12: Leveraging UVM-based Low Power Package Library to SOC Designs
Shikhadevi Katheriya, Silicon Interfaces; **Avnita Pal,** Silicon Interfaces; **Sastry Puranapanda,** Silicon Interfaces

#13: Pragmatic Formal Verification of Sequential Error Detection and Correction Codes (ECCs) used in Safety-Critical Design
Aman Kumar, Infineon Technologies

#14: System-Level Power Estimation of SSDs under Real Workloads using Emulation
Sangmin Kim, Samsung Electronics Co., Ltd.; **Kwanghyo Ahn,** Samsung Electronics Co., Ltd.; **Changhoon Han,** Samsung Electronics Co., Ltd.; **Hyunsik Kim,** Samsung Electronics Co., Ltd.; **Jaewoo Im,** Samsung Electronics Co., Ltd.

#15: UVM Based Mixed-Signal Verification of a Display PMIC Designed for OLED Display Applications
Vijay Kumar, Samsung Semiconductor India Research; **Adnan Malik,** Samsung Semiconductor India Research

#16: Verification Macros: Maintain the integrity of verifiable IP UPF through integration
Amit Srivastava, Synopsys Inc; **Shreedhar Ramachandra,** Synopsys Inc

#17: A HW and SW integrated power optimization approaches with power aware simulations at SOC
Eldin Ben Jacob, Harshal Kothari, Sriram Kazhiyur Soundarrajan, Somasunder Kattepura Sreenath, Samsung Semiconductors India Research

12:30 – 13:30

Lunch Sponsored by Siemens EDA
A Data-Driven Escape from the Verification Pit of Despair
Room: Pine Cedar

SIEMENS

Abstract: A verification crisis is upon us that will not be solved solely through improvements in verification point tools. The solution requires a holistic and philosophical change in the way we approach design with a foundation based on bug prevention combined with collaborative data-driven verification solutions . In this presentation, Harry presents the state of verification today based on the findings from the 2022 Wilson Research Group study and then proposes a novel solution to today's verification crisis.

13:30 – 14:30

Keynote: What Do Farming, Steel, and Space Have in Common?
Room: Oak / Fir
Dirk Didascalou, Chief Technology Officer Siemens Digital Industries

As CTO, Dirk is responsible for the overall technology and architecture strategy for Siemens Digital Industries. He oversees strategic industrial engagements with partners and joint customer initiatives. Additionally, Dirk takes a leading role in the company wide IoT board and is driving digital transformation across all Siemens divisions.

Dirk has two decades of experience in R&D, deep technology expertise in mobile communications, cloud computing and hyperscale architecture, software-as-a-service (SaaS), and IoT solutions. Dr. Didascalou joined Siemens from Amazon Web Services (AWS), where he was Vice President for the Internet of Things, based in Seattle, Washington, USA.

Prior to his time at AWS, Dr. Didascalou worked for Microsoft as Corporate Vice President Technology. He moved to Microsoft with that company's acquisition of Nokia Corp.'s Mobile Phones entity, where he held various leadership positions in Copenhagen, Denmark, and Beijing, China – most recently as the Senior Vice President R&D responsible for worldwide engineering. Dirk holds a Bachelor of Science degree and masters of science degree in Electrical and Electronics engineering, with a Ph.D. in Communications & RF from Karlsruhe Institute of Technology.

Abstract: Well, it's the digital transformation that makes you healthy by eating freshly grown food, takes you to new destinations while relaxing in an autonomous vehicle, and lets you reach for the stars thanks to emission-free space travels.

It may sound too good to be true, but it's already reality. Digitalization has transformed the everyday: The way we live, communicate, travel, and work. Now it's time to turn dreams into reality for a better tomorrow. And we know, chips are the heart of today's digital transformation.

With examples from Space Perspective, 80 Acres Farms, and others, we will show you how the new wave of digitalization is driving huge transformations and can be an inspiration for every industry.

It's about connecting the real and the digital worlds to help everyone innovate faster and adapt to the world better than ever before by turning complexity into competitive advantage. You dream it – let's make it together.

14:30 – 15:00

Coffee Break
Room: Gateway Foyer

15:00 – 17:00

Formal Restrained
Room: Monterey Carmel
Session Chair: **Xiaolin Chen**

FSM Minesweeper – Scalable Formal Verification Methodology for Detecting Hangs in Interacting FSMs
Anshul Jain, Intel Corporation; **Achutha KiranKumar V M,** Intel Corporation; **Harbaksh Gupta,** Intel Corporation; **Shashwat Singh,** Intel Corporation

Doing the Impossible: Using Formal Verification on Packet Based Data Paths
Doug Smith, Doulos

Deadlock Free Design Assurance Using Architectural Formal Verification
Bhushan Parikh, Intel Corporation; **Shaman Narayana,** Intel Corporation

Technical Program: Tuesday, February 28 (cont.)
Time Zone is PST

15:00 – 17:00

Process RISC_V
Room: Oak
Session Chair: **Kamel Belhous**

Automated Thread Evaluation of Various RISC-V Alternatives using Random Instruction Generators
Endri Kaja, Infineon Technologies AG; **Nicolas Gerlin,** Infineon Technologies AG; **Dominik Stoffel,** Technische Universität Kaiserslautern; **Wolfgang Kunz,** Technische Universität Kaiserslautern; **Wolfgang Ecker,** Infineon Technologies AG

RISC-V Security Verification using Perspec/Portable Stimulus
Siyan Li, MediaTek; **Junxia Wang,** Mediatek; **Kiran Kumar Subrahmanya Palla**, Cadence

Random testcase generation and Verification of Debug Unit for a RISCV Processor Core
Sneha Mishra, NXP Semiconductors; **Lu Hao,** NXP Semiconductors; **Ajay Sharma,** NXP Semiconductors; **Afshan Anjum,** NXP Semiconductors; **Lucia Franco,** NXP Semiconductors; **Sourav Roy,** NXP Semiconductors; **Jeff Scott,** NXP Semiconductors

The evolution of RISC-V processor verification: open standards and verification IP
Aimee Sutton, Imperas Software Ltd.; **Lee Moore,** Imperas Software Ltd.; **Mike Thompson,** OpenHW Group

15:00 – 17:00

Systematic Methodology
Room: Fir
Session Chair: **Jeremy Ridgeway**

What I Wish My Regression Run Manager's Vendor Knew!
David Crutchfield, Infineon Technologies; **Brian Craw,** Infineon Technologies; **Jason Lambirth,** Infineon Technologies

Using a modern software build system to speed up complex hardware design
Varun Koyyalagunta, Tenstorrent

Regvue: Modern Register Documentation
Rob Donnelly, NASA Jet Propulsion Laboratory; **Josh Geden,** NASA Jet Propulsion Laboratory

What's Next for SystemVerilog in the Upcoming IEEE 1800 standard
Dave Rich, Siemens EDA

Technical Program: Wednesday, March 1
Time Zone is PST

8:00 – 9:00

Panel: Systems are Evolving. Is Verification Keeping Up?
Room: Oak / Fir

We get so involved in polishing and refining what we know how to do that we sometimes forget to look up. The systems we must verify aren't just getting bigger. Architectures are becoming more sophisticated, as are system standards and value-chain expectations, all to meet the expansive goals we have in the cloud, 5G networks and smart everything. Now systems are splitting across chiplets, boards and wireless networks. All these trends have significant implications for verification and validation.

Products for fast moving markets don't start with a nailed-down specification. Concurrent system design and verification is becoming more common, motivating continuous integration and ICE/digital twin validation. Some IPs come with unique needs: Validating RISC-V implementations to the open ISA standard; Verifying AI accelerators against a meaningful subset of huge test suites; Validating memory consistency in multi-core platforms, all the way to rack-level; Performance verifying NoC/mesh networks under a broad range of traffic demands. Non-functional metrics – power, safety, security – are familiar but becoming more complex, in part in the need to be validated together. FMEDA analysis is necessary but not sufficient for ASIL-D verification, while hacker ingenuity seems boundless (side-channel attacks, speculative execution …).

Verification teams want more application-centric tooling and methodologies to help address these needs. The Innovation in Verification series (published monthly in SemiWiki) was started three years ago to break out of our comfort zone by exploring research papers in hardware, software verification and systems verification and validation. Our goal is to stimulate, in an open forum, new ideas and product advances – to be ready to meet system needs as they appear. Panelists will discuss key problems for which they would like to see breakthroughs and promising ideas/research they would like to see explored further. We welcome audience feedback and ideas in the same vein.

Panelists include:

- **Paul Cunningham,** Senior VP and GM, Cadence System Verification Group
  - Dr. Paul Cunningham has served as Senior Vice President and General Manager of the System Verification Group (SVG) since March 2021, running the division since 2018. His responsibilities include logic simulation, emulation, prototyping, formal verification, Verification IP, and functional debug. Prior to this role, Cunningham was responsible for Cadence's frontend digital design tools including logic synthesis and design-for-test.
- **Raúl Camposano,** CTO Silvaco, Partner at Silicon Catalyst
  - Dr. Camposano is Chief Technology Officer at Silvaco, responsible for driving and managing all software and design IP product development and technology roadmaps. He is also a partner at Silicon Catalyst, an incubator for semiconductor solutions, and lectures on EDA and Machine Learning Hardware at Stanford. He was previously an advisor to Applied Materials and the CEO of Sage Design Automation acquired by Applied Materials in 2020. He was also CEO of Nimbic, acquired by Mentor Graphics in 2014. Raúl spent most of his career with Synopsys, where he served as Chief Technology Officer, Senior Vice President, and General Manager.
- **Dave Kelf,** CEO Breker Systems
  - Dave holds the position of CEO of Breker. Prior to that, as Chief Marketing Officer Dave was responsible for all aspects of Breker's marketing activities, strategic programs and channel management. Earlier, Dave served as vice president of worldwide marketing solutions at formal verification provider OneSpin Solutions. Dave was president and CEO of Sigmatix, Inc. He worked in sales and marketing at Cadence Design Systems, and was responsible for the Verilog and VHDL verification product lines. As vice president of marketing at Co-Design Automation and then Synopsys, Dave oversaw the successful introduction and growth of the SystemVerilog language, before running marketing for Novas Software, noted for the Verdi product line, which became Springsoft and is now part of Synopsys.

Technical Program: Wednesday, March 1 (cont.)
Time Zone is PST

8:00 – 9:00

Panel: Systems are Evolving. Is Verification Keeping Up? (cont.)
Room: Oak / Fir

- **Sujata Ravi,** VP Silicon Verification and Validation, Ampere
  - Sujata has extensive leadership experience in the semiconductor industry in roles ranging from design, pre-silicon verification to post silicon validation and customer support. Prior to joining Ampere, she worked at Intel for 15 years in a variety of positions throughout the company. Most recently, she was responsible for pre-silicon verification with focus on emulation innovation and initiatives to "shift left bug findings" and reduce sample time to customers. While at Intel, Sujata also led a design verification, design automation and emulation team responsible for five generations of Xeon processors. She received an Intel Achievement Award for her work in driving "shift left" initiatives that helped reduce considerable amount of time to product readiness.
- **Alex Starr,** AMD
- **Bernard Murphy,** Advisor and SemiWiki will moderate
  - Dr. Murphy is a freelance advisor and blogger on verification and IP at SemiWiki. Earlier he was VP of Engineering, later CTO at Atrenta (the SpyGlass company) from inception to acquisition by Synopsys.

9:00 – 9:30

Coffee Break
Room: Gateway Foyer

9:30 – 11:00

Discovering Formal
Room: Monterey Carmel
Session Chair: **Erik Seligman**

Demystifying Formal Testbenches: Tips, Tricks, and Recommendations
Shahid Ikram, Marvell; **Mark Eslinger,** Siemens

A Simulation Expert's Guide to Formally Verifying Software Status and Interrupts
Neil johnson, ciena

9:30 – 11:00

Constraining Constraints
Room: Oak
Session Chair: **Dave Rich**

Creating 5G Test Scenarios, the Constrained-Random way
Keshav Kannan, Intel; **Eric Kim,** Intel

Datagen: Python Constrained Random Test Stimulus Framework
Jonathan George, Microsoft; **James Mackenzie,** Microsoft

See the forest for the trees – How to effectively model and randomize a directed rooted tree structure
Harry Duque, Axis Communications AB; **Lars Viklund,** Axis Communications AB

Technical Program: Wednesday, March 1 (cont.)
Time Zone is PST

9:30 – 11:00

Completing Coverage
Room: Fir
Session Chair: **Progyna Khondkar**

Improve emulator test quality by applying synthesizable functional coverage
Hoyeon Hwang, Samsung Electronics; **Teaseong Kim,** Samsung Electronics; **Sanghyun Park,** Samsung Electronics; **Yong-Kwan Cho,** Samsung Electronics; **Dohyung Kim,** Samsung Electronics; **Wonil Cho,** Samsung Electronics; **Sanggyu Park,** Samsung Electronics

Closing Functional Coverage With Deep Reinforcement Learning – A Compression Encoder Example
Eric Ohana, Queensland University of Technology, Australia – University of Bielefeld, Germany

GraphCov: RTL Graph Based Test Biasing for Exploring Uncharted Coverage Landscape
Debarshi Chatterjee, Nvidia Corporation; **Spandan Kachhadia,** Nvidia Corporation; **Chen Luo,** Nvidia Corporation; **Kumar Kushal,** Nvidia Corporation; **Siddhanth Dhodhi,** Nvidia Corporation

11:00 – 12:00

Poster Ninja Warrior
Room: Oak

12:00 – 13:30

Lunch Sponsored by Accellera System Initiative
Brief update on Accellera working group activities, followed by an invited talk: "RISC-V Everywhere"
Room: Pine Cedar
Presented by Mark Himelstein, CTO RISC-V International

Before RISC-V international Mark Himelstein was the President of Heavenstone, Inc. which concentrated on Strategic, Management, and Technology Consulting providing hardware and software product architecture, analysis, mentoring and interim management. Previously, Mark started Graphite Systems, Inc (acquired by EMC) where he was the VP of Engineering and CTO developing large Analytics Appliances using highly integrated FLASH memory. Prior to Graphite, Mark held positions as the CTO of Quantum Corp, Vice President of Solaris development engineering at Sun Microsystems and other technical management roles at Apple, Infoblox, and MIPS. Mark has a bachelors degree in Computer Science and Math from Wilkes University in Pennsylvania and a mastersdegree in Computer Science from University of California Davis/Livermore. In addition to publishing numerous technical papers and holding many patents, he is the author of the book "100 Questions to Ask Your Software Organization".

Technical Program: Wednesday, March 1 (cont.)

Time Zone is PST

13:30 – 14:30

Panel: AI-ML Algorithms are Transforming Verification: Separating Hype from Reality

Room: Oak / Fir

In this panel, a few verification executives from leading EDA-IP and semiconductor/systems companies will discuss state of the art of their design verification environments that power the new generation of advanced processors and systems which could potentially change the semiconductor landscape. These include verifying IPs, System-on-Chips (SoCs), System-of-Chips and System-of-Systems for 5G-6G, Cloud and Edge Computing and AI-ML in emerging and growing verticals including Autonomous Vehicles, HealthTech, Mil-Aero, HPC and more.

Some of this discussion will center around the reality behind AI-ML algorithms to transform verification/validation and system-level testing of such systems. Are we there yet? What will it take to make these systems really work for us? Is AI-ML sufficient? What kind of standards will we need to make it all work?

Here are some among many open challenges that we would like our panelists to address:

- **What does it take to verify chips, SoCs and systems for 5G-6G, Edge computing and AI-ML?**
- **UVM, ISO26262, DO-254, Python: what next? How best can we verify software-driven hardware, system-of-systems? What kind of standards would we need beyond these?**
- **How do we verify with emerging metrics beyond functionality? How do we deal with increasing complexity?**
  - Functional safety, security, Performance per watts, SLM
- **At what step do AI-ML algorithms help in pre- and post-silicon verification?**
  - Will they replace or complement formal approaches?
  - Can they help us in scaling with heterogeneous architectures using chiplets to create System-of-Chips and System-of-Systems?
- **Are there any limitations to the use of AI-ML algorithms?**
  - What will it take to get to our longer-term vision of predictable RTL and Gate-level signoff, and first-pass Silicon?

Moderator:

Shankar Hemmady, Blue Horizons

Panelists:

Prith Banerjee, CTO, Ansys

William Hung, Vice President of Engineering, Cadence

Saad Godil, Director of Applied Deep Learning Research, Nvidia

Manish Pandey, VP R&D & Fellow, Synopsys

Jean-Marie Brunet, VP and GM of Hardware-Assisted Verification, Siemens

14:30 – 15:00

Coffee Break

Room: Gateway Foyer

Technical Program: Wednesday, March 1 (cont.)
Time Zone is PST

15:00 – 16:30

Analog/Mixed Signal Smorgasbord
Room: Monterey Carmel
Session Chair: **Shekar Chetput**

Take AIM! Introducing the Analog Information Model
Chuck McClish, Microchip Technology Inc.

Automated Modeling Testbench Methodology Tested with four Types of PLL Models
Jun Yan, Renesas Electronics; Josh Baylor, Renesas Electronics

SystemVerilog Real Models for an In-Memory Compute Design
Daniel Cross, Cadence Design Systems

15:00 – 16:30

Protecting Safety and Security
Room: Oak
Session Chair: **Nagi Naganathan**

Is Your System's Security preserved? Verification of Security IP integration
Predrag Nikolic, Veriest Solutions

Complex Safety Mechanisms Need Interoperability for Validation and Close Loop for Final Metrics
Daeseou Cha, Samsung; **Vedant Garg,** Siemens EDA; **Ann Keffer,** Siemens EDA; **James Kim,** Siemens EDA; **Woojoo Space Kim,** Samsung Electronics

Early Detection of Functional Corner Case Bugs using Methodologies of the ISO 26262
Moonki Jang, Samsung Electronics; **Sunil Roe,** Samsung Electronics; **Youngsik Kim,** Samsung Electronics; **Seonil Brian Choi,** Samsung Electronics

15:00 – 16:30

UVM Buffet
Room: Fir
Session Chair: **Srivatsa Vasudevan**

It's Not Too Late to Adopt: The Power of UVM
Kathleen Wittmann, Rockwell Automation

UVM-SV Feedback Loop – The foundation of self-improving testbenches
Andrei Vintila, AMIQ Consulting; **Sergiu Duda,** AMIQ Consulting

Verifying RO registers: Challenges and the solution
Ivana Dobrilovic, Veriest Solutions

16:30 – 17:00

Break

17:00 – 17:30

Best Paper Presentation
Room: Bayshore Ballroom

17:30 – 18:30

Reception
Room: Bayshore Ballroom

Technical Program: Thursday, March 2
Time Zone is PST

9:00 – 12:30

Tutorial: Evolutionary and Revolutionary Innovation for Effective Verification Management & Closure
Room: Siskiyou
Presented by Siemens EDA

By: **Darron May,** Siemens EDA; **Mark Carey,** Siemens EDA; **Joseph Hupcey,** Siemens EDA

Abstract: This tutorial will cover the evolution of features and tools to provide efficiency and acceleration to the verification process as well as the revolution required to take full advantage of collaboration, traceability, and emerging technologies provided by machine learning (ML) and virtually unlimited cloud computing resources.

What you will learn:

- How to enhance your current D&V workflow with proven collaboration, requirements traceability, coverage tracking, regression management, and more as inspired by proven technologies from the software world
- How verification planning tools can be integrated with lifecycle management flows by taking advantage of the Open Services for Lifecycle Collaboration standard.
- How ML can be applied to the analysis of the coverage model using analytical navigation to speed understanding and accelerate closure, how ML can complement rules-based systems to improve regression efficiency and debug turn-around times, and how this enables a shift from descriptive to prescriptive analytics with full visibility of the status of projects
- What is required to take full advantage of this kind of massive compute resource scalability with respect to both dynamic reaction and streaming data.

9:00 – 10:30

Workshop: Verification 2.0 – Multi-Engine, Multi-Run AI-Driven Verfication
Room: Cascade
Presented by Cadence

By: **Matt Graham,** Cadence

Abstract: Growth in complexity of ICs, particularly SoCs, continues at a pace that will cause verification requirements to out run engineering capacity, compute capacity and tool performance. A new generation of EDA tools must emerge, leveraging big data and deploying AI across multiple runs of multiple engines to enable a dramatic increase in overall productivity.

The recently announce Cadence Verisium AI-Driven Verification platform is a suite of applications that represents just such a generational shift for verification campaigns. The Verisium platform, built on the Cadence Joint Enterprise Data and AI (JedAI) Platform provides capabilities that truly reduce silicon bugs and accelerates time to market.

In this session, we will highlight how a shift to multi-run, multi-engine solutions can address the continued increase in the effort required to close verification. The application of big data and AI to the verification problem will also be introduced, with particular emphasis on its application to debug. A number of the apps from the Verisium Platform will be reviewed, along with some insight into their leveraging of multiple engines (Japser Formal, Xcelium Logic Simulation) and their connections to multiple data sources (waveforms, RTL, coverage and revision control data).

Finally, we'll review some of the results that users of such technologies are experiencing, and discuss some of the future potential of these technologies.

9:00 – 10:30

Workshop: Accelerate Coverage Closure from Day-1 with AI-driven Verification

Room: Donner

Presented by Synopsys

By: **Malay Ganai,** Synopsys; **Will Chen,** Synopsys; **Srikanth Vadanaparthi,** Synopsys

Abstract: Functional verification dominates semiconductor development, consuming the largest percentage of project time and resources. Verification engineers use various criteria such as bug rates and coverage metrics or at least asymptotically converge toward target goals to determine when to signoff.

In this workshop, we present a new and differentiating AI-driven verification technology, known as Intelligent Coverage Optimization (ICO). The workshop will demonstrate how verification engineers can benefit from early adoption of ICO's simple use model to accelerate coverage convergence in simulation, expose bugs early in the design cycle, reduce debug effort and improve verification turnaround time, thereby maximizing project resource utilization while reducing the verification schedule. ICO leverages modern artificial intelligence (AI) and machine learning (ML) technologies to help optimize coverage and stabilize the testbench. Through continuous feedback, the testbench is stabilized faster with each verification cycle and as more project experience is accumulated.

We will present real case studies showing how the entire verification process shifted left using ICO early in the cycle. Employing AI-driven verification techniques reduced the manual effort to write directed tests, helping find bugs faster, and required fewer regression iterations to reach the target metrics, saving several weeks of effort and up to 15% reduced peak demand of grid resources.

10:30 – 11:00

Coffee Break

Room: Bayshore Foyer

11:00 – 12:30

Workshop: A Wholistic Approach to Optimizing Your System Verification Flow

Room: Cascade

Presented by Cadence

By: **Ross Dickson,** Cadence

Abstract: For years the challenges facing the design and verification engineers have been growing following the increase in design complexity due to Moore's law. Luckily EDA has managed to keep up with this complexity though innovations in verification tooling. While the correlation between these trends have keep us all employed delivering high quality products, the industry is currently in the process of navigating a discontinuity in complexity due to software. Traditionally RTL verification has been relatively insulated from the complexity of software which has also been growing with Moore's law, this isolation has been crumbling as the software becomes more critical to the success of the device. In this workshop we will present best practices in how a unified co-verification flow can address this discontinuity in verification complexity though integration of tools and unification of UI for the previously separate verification domains.

11:00 – 12:30

Workshop: Growing need for End-to-end Protocol Verification Solutions from IP to Multi-die Systems

Room: Donner

Presented by Synopsys

By: **Varun Agrawal,** Synopsys

Abstract: With ever-increasing chip design complexity, including chips for domain-specific applications, the role of on-chip and off-chip protocols have increased drastically. Protocol versions are evolving very rapidly to meet application needs for bandwidth, latency, and coverage. Verifying these protocols for behavior, performance, and power in actual application payloads and usage scenarios is absolutely necessary.

In this workshop, we will discuss how protocol verification is becoming more and more challenging as designs evolve from IP blocks to multi-die system setups and why IP verification is no longer enough. An end-to-end protocol is essential to validate protocol behavior and fulfill verification requirements for IP through system designs. We will walk through uses cases for when to apply virtual models, speed adapters, virtual transactors, and protocol interface cards to exercise interfaces from IP to systems. We will also discuss various power, performance, and pre-to-post silicon continuity use cases that are enabled with an end-to-end protocol verification solution.

12:30 – 13:30

Lunch Sponsored by Accellera System Initiative
UVM 1800.2-2020-2.0 Library Discussion

Room: Sierra

Presenters from the UVM Working Group

By: **Srivatsa Vasudevan,** Intel; **Jamsheed Agahi,** Arteris

Abstract: UVM Working Group members will discuss the release of the 1800.2-2020-2.0 library. Presenters will focus on the implementation of the IEEE 1800.2-2020 standard to the library, with greatly enhanced backward-compatibility using code written for UVM1.1d or UVM1.2, creating some substantial performance improvements. Questions from attendees are welcome.

13:30 – 15:00

Tutorial: Harnessing the Power of UVM for AMS Verification with XMODEL

Room: Siskiyou

Presented by Scientific Analog

By: **Jaeha Kim,** Scientific Analog; **Charles Dancak,** Scientific Analog

Abstract: In this tutorial, you will learn how to write a UVM testbench for analog/mixed-signal circuits. UVM (Universal Verification Methodology) is a framework of standardized SystemVerilog classes for building reusable and scalable testbenches for digital systems, and we will show that it can be extended to verifying analog circuits simply by using a well-defined fixture module encapsulating the device-under-test (DUT) and its AMS instrumentations described with XMODEL primitives. Through a series of hands-on lab exercises using a digitally-programmable audio bandpass filter as an example, you will learn how to write a UVM testbench that measures the filter's transfer gains at randomly-chosen frequencies and collects the results in a scoreboard.

The tutorial is organized in two parts. The first part introduces XMODEL as a way of modeling and simulating analog circuits in SystemVerilog. The lab exercises will show how to auto-extract a SystemVerilog model from the analog filter circuit and build a SystemVerilog testbench measuring its response to a sinusoidal input using XMODEL primitives. By the end of the first part, you will have your fixture module enclosing the analog DUT and its instrumentations ready.

The second part starts with an intuitive overview of UVM and shows how to put the sequencer, driver, monitor, and scoreboard components around the fixture module to build a UVM testbench. The lab exercises will guide you how to write a sequencer generating a sequence of random frequencies, a driver sending the stimulus data to the fixture module, a monitor receiving the measured responses from the fixture, and finally a scoreboard comparing the results against the SPICE simulation data. By the end of this second part, you will be running simulation with your own UVM testbench verifying the filter's transfer gains at randomly-chosen frequencies.

No strong background is required either in analog circuits or digital verification. Each concept, feature, or technique is introduced in a step-by-step fashion and anyone with a basic knowledge of SystemVerilog is welcome to attend.

13:30 – 15:00

Workshop: Verification of Inferencing Algorithm Accelerators

Room: Donner

Presented by Siemens EDA

By: **Russel Klein,** Siemens EDA

Abstract: This short workshop will cover the verification of a custom AI accelerator as it is migrated from a machine learning framework in Python to RTL. Using High-Level synthesis provides a C++ version of the algorithm being verified. We will show how the original Python can be verified, and subsequent implementations, C++ and RTL, can be shown to be equivalent to the original Python. This allows for greater verification at the algorithmic level, thus requiring less verification at the RTL level. Please see attached proposal.

13:30 – 15:00

Workshop: Understanding the RISC-V Verification Ecosystem

Room: Donner

Presented by Imperas

By: **Aimee Sutton, Simon Davidmann, Kevin McDermott,** Imperas

As RISC-V processor technology continues to gain traction the practice of RISC-V processor functional verification is advancing and evolving. What started as a nebulous task with knowledge and proprietary best practices confined within a few commercial organizations is now changing. Today there are various methodologies and tools publicly available that can be selected based on the verification quality objectives of the project. Tools and techniques have evolved so that it's no longer necessary to build it all yourself or reinvent the wheel. There are resources to help get started, from open-source examples to commercial offerings such as RISC-V processor verification IP.

This tutorial will help the audience understand and navigate the RISC-V verification ecosystem. Some of the topics covered include:

- Understanding the tools used in RISC-V processor verification: instruction set simulators, processor reference models, random instruction stream generators, verification IP
- Compare and contrast techniques that can be used for RISC-V processor verification: post-simulation trace compare, self-checking tests, lockstep co-simulation, functional coverage
- Open standards for RISC-V processor verification: RISC-V Verification Interface (RVVI)
- Open-source examples and commercial offerings

At the conclusion the audience will leave the information needed to make a decision about the best solution for their RISC-V processor verification project.

15:00 – 15:30

Coffee Break

Room: Bayshore Foyer

15:30 – 17:00

Workshop: Virtio based GPU Modeling

Room: Cascade

Presented by Vayavya Labs

By: **Pratik Parvati, Karthick Gururaj -** Vayavya Labs

Abstract: Simulating a full-blown GPU is complex and challenging and demands parallel simulators as sequential simulators are slow. GPU has hundreds and thousands of processing elements on a single GPU die; simulating such environments asks for a challenging approach.

But instead, if we can leverage the Host CPU and GPU resources; we can offload such complexities to the GPU hardware with a minimalistic SystemC (or equivalent) model running on a Host CPU.

One approach to achieve this is using virtio-based GPU modeling. In this workshop, we dive deep into technical details to model the GPU simulator using SystemC.

15:30 – 17:00

Workshop: Getting Beyond ISA Compliance: Advanced Core/SoC Verification for RISC-V and other Beasts

Room: Donner

Presented by Breker Systems

By: **Adnan Hamid,** Breker Systems

Abstract: Processor core verification represents an array of complex challenges. With the advent of RISC-V, new issues have emerged, which add to this complexity. Whether you are a processor developer working on a RISC-V or other core, or an SoC integrator incorporating one of these new processors, the learning we will provide in this workshop will add to your arsenal of verification techniques.

Breker has been working with multiple RISC-V vendors and users. We have discovered that tests used to ensure the smooth integration of these processors into SoCs, both large and small, may also be applied to cores under development in unique ways to drive increased quality. For example, interrupt testing at the SoC level may also be applied to the core to ensure the smooth handling of the operational interrupt. Load Store mechanisms at the SoC level may be introduced at the core level to understand if the device can be tripped up. Will the RISC-V memory protection be enough to ensure security at the SoC level? Of course for multiple core or application devices, full system coherency becomes a critical component.

What are the algorithms that may be effectively used to provide these tests? How do you ensure full coverage of multi-faceted tests? How can you torture test the core and SoC to tease out complex, hard to predict corner cases in which might lurk a bug or an operational bottleneck? All of these questions will be answered during this workshop.

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